REMARKS

Claims 1-10, 12, 14, and 19-20 are pending.

Claims 1-10, 12, 14, and 19-20 have been rejected under 35 U.S.C. 103 as being unpatentable over Paradine et al., U.S. Patent No. 6,049,565 ("Paradine") in view of Hirata, U.S. Patent No. 5,327,391 ("Hirata") and further in view of Matsumoto, U.S. Patent No. 5,812,944 ("Matsumoto"). Applicants respectfully submit that the claimed invention is not taught, suggested or implied by Hirata, Paradine, or Matsumoto, either singly or in combination.

As discussed in the Specification, and in response to the previous Official Action, the present invention relates to a system and method for rate adjustment. A rate adjustment system according to an embodiment of the invention includes a first jitter buffer pair and a second buffer pair. The buffers in the first and second jitter buffer pairs are swapped to effect a rate adjustment. In particular, the buffers in the pairs are alternately filled at a first clock rate and emptied at a second. The swapping occurs simultaneously at the second clock rate. In some embodiments, the first cock is associated with a sample clock frequency and the second clock is associated with a frame clock frequency.

In contrast, contrary to the suggestion in the Official Action, none of the references relate to simultaneously swapping pairs of buffers as generally recited in the claims at issue. Further, none of the references provide that a first clock frequency is associated with a sample clock and a second is associated with a frame clock, as generally recited in the claims at issue.

As discussed in response to the previous Official Action, while Paradine provides a double buffer 320 and a double buffer 330, the halves of the double buffers are never alternated or swapped. Instead, samples are passed into one half of the buffer and read out of the other. No swapping of halves occurs. **Thus, nothing remotely resembling alternation of buffers occurs in Paradine.**

Hirata similarly fails to disclose, .e.g, as recited in claim 1, "wherein said first or second jitter buffers alternately fill at said first clock frequency and empty at said

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second clock frequency, and said third or fourth jitter buffers alternately fill at said second clock frequency and empty at said first clock frequency, wherein alternation between said first and second jitter buffers and said third and fourth jitter buffers occurs simultaneously at said second clocking frequency, said first clocking frequency associated with a sample clock, said second clocking frequency associated with a frame clock."

As discussed above, according to embodiments of the present invention, one pair of buffers operates in a first "direction" and the other operates in a second "direction." That is, the first pair is filled at a first clock and emptied at a second clock rate. The second pair is filled at the second clock rate and emptied at the first. The individual buffers in the pairs are simultaneously swapped at the second clock rate. Thus, both oppositely directed pairs are swapped according to the same clock rate. In some embodiments, the rate at which the buffers are swapped is a frame clock rate.

In contrast, Hirata provides a first data memory 24-1 and a second data memory 24-2. Usage of the first and second data memories is governed by selector 23. First generating circuit 21 provides input to write in counters 25-1 and 25-2 and second signal generating circuit provides input to read-out counters 26-1 and 26-2. Receive clock 101 is provided to the counters 25-1 and 25-2; receive clock 103 is provided to counter 26-1 and 26-2. Clocks 101 and 103 clock the read in and write out, respectively.

To the extent that there is alternation in Hirata, it occurs at the frame rate (See, e.g., Col. 4, lines 17-21 and Col. 4, lines 39-44)(reset signals 106, 107 are provided in response to the frame clock pulse 102; reset signals 111, 112 are provided at frame clock pulse 104, which is the same rate as frame pulse 102, but may have different phase) while the read out and the write in both occur at the system clock rate (101 and 103 are at the same frequency though may have a different phase). That is, in Hirata, the read and write occur at the same rate, and the alternation between first and second memory occurs at the different frame rate.

However, in the present invention, the swapping of the buffers occurs at the frame clock rate, which is also one of the rates at which the buffers are read in or out of (the other being the sample clock rate). That is, in the present invention, the buffers in

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each pair alternately fill and empty at the sample and/or frame clock rates, while the
rate of alternation is the frame clock rate. In contrast, in Hirata, alternation occurs at
the frame clock rate, while both read out and write in occur at the same system clock
rate.

Matsumoto is relied on merely for allegedly illustrating a block oriented encoding
scheme. However, like Hirata and Paradine, Matsumoto fails to teach alternately
swapping buffers according to frequencies as generally recited in the claims at issue.

As such, the Examiner is respectfully requested to reconsider and withdraw the
rejection of the claims.

For all of the above reasons, Applicants respectfully submit that the application is
in condition for allowance, which allowance is earnestly solicited.

PLEASE MAIL CORRESPONDENCE TO: Respectfully submitted,

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